JC10 Rec'd PCT/PTO 26 FEB 2002

FORM PTO-1390 (REV. 12-2001) U S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: MAF0004.US

U S APPLICATION NO (If known, see 37 CFR 1.5): 10/069637

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/IB00/01306	25 August 2000	27 August 1999

TITLE OF INVENTION FILTER DEVICE COMPRISING A CORE FILTER, A DECIMATOR AND AN INTERPOLATOR

APPLICANT(S) FOR DO/EO/US
Heinz G. Goeckler, et al.

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [X] This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. [ ] This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. [ ] This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. [ ] The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. [X] A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. [X] is attached hereto (required only if not communicated by the International Bureau).
   b. [ ] has been communicated by the International Bureau.
   c. [ ] is not required, as the application was filed in the United States Receiving Office (RO/US).
6. [X] An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. [X] is attached hereto.
   b. [ ] has been previously submitted under 35 U.S.C. 154(d)(4).
7. [ ] Amendments to the claims of the International Aplication under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. [ ] are attached hereto (required only if not communicated by the International Bureau).
   b. [ ] have been communicated by the International Bureau.
   c. [ ] have not been made; however, the time limit for making such amendments has NOT expired.
   d. [ ] have not been made and will not be made.
8. [ ] An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371 (c)(3)).
9. [X] An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. [ ] An English lanugage translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 20 below concern document(s) or information included:

11. [ ] An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. [ ] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. [X] A FIRST preliminary amendment.
14. [ ] A SECOND or SUBSEQUENT preliminary amendment.
15. [ ] A substitute specification.
16. [ ] A change of power of attorney and/or address letter.
17. [ ] A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
18. [ ] A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. [ ] A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. [X] Other items or information:

Form PCT/RO/101
Form PCT/ISA/210

10069637 .052802
JC19 Rec'd PCT/PTO 26 FEB 2002

U.S. APPLICATION NO (if known, see 37 CFR 1.5) 10/069637	INTERNATIONAL APPLICATION NO PCT/IB00/01306	ATTORNEY'S DOCKET NUMBER MAF0004.US

21. [X] The following fees are submitted:	CALCULATIONS	PTO USE ONLY
BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)):		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **$1040.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **$890.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$740.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$710.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) **$100.00**		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 890.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than [ ] 20 [X] 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$ 130.00	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	$	
Total claims	11 - 20 =		x **$18.00**	$ 0.00	
Independent claims	1 - 3 =		x **$84.00**	$ 0.00	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ **$280.00**	$ 0.00	

TOTAL OF ABOVE CALCULATIONS =	$1,020.00	
[ ] Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.	$ 0.00	
SUBTOTAL =	$1,020.00	
Processing fee of **$130.00** for furnishing the English translation later than [ ] 20 [ ] 30 months from the earliest claimed priority date (37 CFR 1.492(f)).	$ 0.00	
TOTAL NATIONAL FEE =	$1,020.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +	$ 0.00	
TOTAL FEES ENCLOSED =	$1,020.00	
	Amount to be refunded:	$
	charged:	$

a. [X] A check in the amount of $ 1,020.00 to cover the above fees is enclosed.

b. [ ] Please charge my Deposit Account No. __________ in the amount of $ __________ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. [X] The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 20-0095 . A duplicate copy of this sheet is enclosed.

d. [ ] Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137 (a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Todd T. Taylor, TAYLOR & AUST, P.C.
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P.O. Box 560
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Todd T. Taylor
SIGNATURE

Todd T. Taylor
NAME

36,945
REGISTRATION NUMBER

"EXPRESS MAIL COVER LETTER" 10/069637
U.S. PATENT APPLICATION
JC19 Rec'd PCT/PTO 26 FEB 2002

Date: February 26, 2002

Commissioner for Patents
Box PCT
Washington, DC 20231

Re: Application for United States Letters Patent

APPLICANT: Heinz G. Goeckler, et al.

TITLE OF INVENTION: FILTER DEVICE COMPRISING A CORE FILTER, A DECIMATOR AND AN INTERPOLATOR

Sir:

Forwarded herewith is the above-identified application, consisting of the following:

Form PTO 1390
International Application (PCT/IB00/01306)
Specification (7 Sheets)
Claims (2 Sheets)
Drawings (5 Sheets)
Declaration ___ Executed _X_ Unexecuted
Assignment___ Yes _X_ No
Information Disclosure Statement __ Yes _X_ No
English Translation
Form PCT/RO/101 (English)
Form PCT/ISA 210 (English)
Preliminary Amendment

Respectfully submitted,

Todd

Todd T. Taylor
Registration No. 36,945
Attorney for Applicant

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"EXPRESS MAIL" Mailing Number EL714259735US

Date of Deposit February 26, 2002.

I hereby certify that this paper or fee is being deposited with the United States Postal Service "EXPRESS MAIL POST OFFICE TO ADDRESSEE" service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Box PCT Washington, DC 20231

Traci D. Johnson
(Typed Name of Person Mailing Paper or Fee)

Traci D. Johnson
(Signature of Person Mailing Paper or Fee)

PATENT

THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	)	
Heinz G. Goeckler, et al.	)	Group:
Serial No.:	)	
Filed: February 26, 2002	)	
PCT No.: PCT/IB00/01306	)	
Int. Filing Date: August 25, 2000	)	Examiner:
Priority Date: August 27, 1999	)	
Title: FILTER DEVICE COMPRISING A CORE	)	
FILTER, A DECIMATOR AND AN INTERPOLATOR	)	

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Sir:

Please enter the following Amendment to the application prior to calculating the filing fee.

Attached hereto as "ATTACHMENT A" is a marked-up copy showing the changes made to the above-identified patent application by the present Amendment.

IN THE CLAIMS

Please substitute the following amended claims 3-7 and 9-11 for original claims 3-7 and 9-11:

3. (Amended) A filter device in accordance with claim 1, characterized in that the core filter (1) is converted into L differently time-delayed filters which are broken down into poly-phase components so that it can be combined with the decimator (2) or the interpolator (3).

4. (Amended) A filter device in accordance with claim 1, characterized in that the system equivalent to the core filter (1) can be operated with a clock rate of f_a/M.

5. (Amended) A filter device in accordance with claim 2, characterized in that the decimator (2) or the interpolator (3) are rearranged relative to the parallel paths with respect to the poly-phase components of the core filter (1) such that the normally necessary commutators (4, 5)

for forwarding sampling values to the core filter (1) can be omitted.

6. (Amended) A filter device in accordance with claim 1, characterized in that both the decimator (2) and the interpolator (3) as well as, optionally, the core filter (1) are set to be operated at a uniform sampling rate.

7. (Amended) A filter device in accordance with claim 1, characterized in that an optimum is selected for the sampling rate change factor R = L/M at which a minimum of computing effort arises for the digital filtering, with this computing effort in particular being characterized as filter operations per unit of time.

9. (Amended) A filter device in accordance with claim 1, characterized in that FIR filter structures, in particular of a non-recursive kind, are used for the core filter (1) and for the decimator (2) and the interpolator (3).

10. (Amended) A filter device consisting of a plurality of cascaded stages, characterized in that every stage is formed as a filter device in accordance with claim 1.

11. (Amended) A filter device in accordance with claim 10, characterized in that the filter device has a central stage.

REMARKS

In the event Applicants have overlooked the need for an extension of time, an additional extension of time, payment of fee, or additional payment of fee, Applicants hereby conditionally petition therefor and authorize that any charges be made to Deposit Account No. 20-0095, TAYLOR & AUST, P.C.

Should any question concerning any of the foregoing arise, the Examiner is invited to telephone the undersigned at (260) 897-3400.

Respectfully submitted,

Todd T. Taylor
Registration No. 36,945

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Enc.: Return postcard

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231, on: February 26, 2002.

Todd T. Taylor, Reg. No. 36,945
Name of Registered Representative

Signature

February 26, 2002
Date

PATENT

Title: FILTER DEVICE COMPRISING A CORE FILTER, A DECIMATOR AND AN INTERPOLATOR
Application Serial No.: Group: Examiner:

ATTACHMENT A:
MARKED-UP COPY SHOWING AMENDMENTS

IN THE CLAIMS

Please substitute the following amended claims 3-7 and 9-11 for original claims 3-7 and 9-11:

3. (Amended) A filter device in accordance with claim 1 [or claim 2], characterized in that the core filter (1) is converted into L differently time-delayed filters which are broken down into poly-phase components so that it can be combined with the decimator (2) or the interpolator (3).

4. (Amended) A filter device in accordance with [any one of claims 1 to 3] claim 1, characterized in that the system equivalent to the core filter (1) can be operated with a clock rate of f_a/M.

5. (Amended) A filter device in accordance with [any one of claims 2 to 4] claim 2, characterized in that the decimator (2) or the interpolator (3) are rearranged relative to the parallel paths with respect to the poly-phase components of the core filter (1) such that the normally necessary commutators (4, 5) for forwarding sampling values to the core filter (1) can be omitted.

6. (Amended) A filter device in accordance with [any one of claims 1 to 5] claim 1, characterized in that both the decimator (2) and the interpolator (3) as well as, optionally, the core filter (1) are set to be operated at a uniform sampling rate.

7. (Amended) A filter device in accordance with [any one of claims 1 to 6] claim 1, characterized in that an optimum is selected for the sampling rate change factor R = L/M at which a minimum of computing effort arises for the digital filtering, with this computing effort in particular being characterized as filter operations per unit of time.

Title: FILTER DEVICE COMPRISING A CORE FILTER, A DECIMATOR AND AN INTERPOLATOR
Application Serial No.: Group: Examiner:

9. (Amended) A filter device in accordance with [any one of claims 1 to 8] claim 1, characterized in that FIR filter structures, in particular of a non-recursive kind, are used for the core filter (1) and for the decimator (2) and the interpolator (3).

10. (Amended) A filter device consisting of a plurality of cascaded stages, characterized in that every stage is formed as a filter device in accordance with [any one of claims 1 to 3] claim 1.

11. (Amended) A filter device in accordance with claim 10, characterized in that the filter device has a central stage [which is formed in accordance with any one of claims 4 to 9].

DECLARATION

I, Jeffrey C. Barfield, of Ahornstrasse 17, 82377 Penzberg, Germany, do hereby declare that I am conversant with the English and German languages and that I am a competent translator thereof.

I verify that the attached English translation is a true and correct translation of the PCT patent application with the international file reference

PCT/IB00/01306

and the international publication number

WO 01/17108 A1.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: February 21, 2002

Jeffrey C. Barfield

FILTER DEVICE COMPRISING A CORE FILTER, A DECIMATOR AND AN INTERPOLATOR

The invention starts from a filter device consisting of a core filter and also of a decimator at the input side and of an interpolator at the output side.

For low-pass filters whose limit frequency is substantially below half the sampling frequency, it is known from [1] N. Fliege "Multiraten-Signalverarbeitung" (Multi-rate signal processing), Teubner-Verlag, Stuttgart, 1993, pages 14 to 146, to first reduce the input sampling rate, then to carry out the actual filtering in a so-called core filter and subsequently to restore the original input sampling frequency by interpolation.

It is known from US 4,725,972 [2] to use parallel filter paths in methods for the matchingn of systems of different sampling rates. The source signal is cyclically distributed to the parallel filter paths and filtered. The signal combination takes place with a commutator and a summing device.

It is possible with the measures of claim 1, to carry out a filtering for which the effort involved – filter operations per unit of time – can be kept low irrespective of the choice of the clock rate of the core filter. In contrast to [1], where the overall computing effort cannot be ideally minimized due to the poor approximation of the optimum decimation factor by an integer-based sampling rate conversion, a minimum computing effort is obtained for the rational decimation factor in accordance with the invention. More-

over, the integer-based approach of the sampling rate reduction in [1] cannot be used when, for example, $f_s > f_a/4$ applies to the cut-off limit frequency f_s in the case of a low-pass filter. In this case, the decimation factor must be $M < 2$, that is not an integer. No effort reduction can evidently be achieved in accordance with [1] for this case, which applies accordingly to high-pass and band-pass filters. The solution in accordance with the invention is, in contrast, free of such limitations. A further advantage of the invention consists of the free selectability of the clock rate at which the system operates, irrespective of the sampling rate. This is made possible by a structure transformation. Thus, its use also does not fail due to technological limits as it does with the direct filtration and in the system proposed in [1].

Advantageous embodiments are shown in the dependent claims.

If the sampling rate f_a*L/M of the core filter cannot be realized for technological reasons, the core filter can be combined by means of transposition and poly-phase break down either with the L/M decimator or with the L/M interpolator whose computing operations are preferably carried out with a uniform sampling rate $f_a/M = f_k/L < f_k$. The selection of the sampling rate change factor $R = L/M$ can be optimized to a minimum computing effort. Once this optimum is fixed, then the sampling rate for the parallelized filter paths of the decimator, interpolator and core filter polyphase components can be selected as desired by a change of the natural numbers L and M in the same sense, without the overall effort being changed.

The invention will be described in more detail with reference to the drawings.

There are shown

Figure 1 a multi-rate FIR filter structure in accordance with the prior art;

Figure 2 the computing effort in dependence on the sampling rate change factor;

Figure 3 a multi-rate FIR filter structure in accordance with the invention;

Figure 4a a filter structure comprising computation efficient decimators and interpolators;

Figure 4b a computation efficient decimator or interpolator for the fractional sampling rate conversion;

Figure 5 a section from Figure 4: output commutator of the decimator, core filter and input commutator of the interpolator;

Figure 6 a filter structure in which the core filter is displaced into the branches of the commutator and is combined with the delays there;

Figure 7a and Figure 7b a filter structure with commutation of the expansion and the core filtration;

Figure 8 an optimized filter structure with adjustable sampling rate; and

Figure 9 a multi-stage filter device in accordance with the invention.

Before looking at the actual realization in accordance with the invention, a solution of the prior art in accordance with [1] will be explained for better understanding.

In accordance with Figure 1, an FIR filter implementation for the sampling rate transformation by the factor M in the form of an integer consists of a decimator 2 at the input side, of a core filter 1 and of an interpolator 3 at the output side. The letter H designates the transfer function of the decimator 2, the letter G designates the transfer function of the interpolator 3 and the letter D' designates the transfer function of the core filter 1. In this connection, the number of multiplications per unit of time determines the computing effort C of the filter structure. This computing effort C is, as Figure 2 shows, a function of the sampling rate change factor $R = 1/M$. The optimum sampling rate change factor can be determined in accordance with [1]. In the case of integer-based sampling rate transformation, R_{opt} can only be roughly approximated in accordance with $R_{opt}=1/M$. In certain applications, the optimum sampling rate factor cannot be described accurately enough by this approximation, cf. also Figure 2. It must be stated that the multi-rate FIR filter structure in accordance with Figure 1 is limited to filter cut-off frequencies $f_s < f_a/4$, where f_a = input sampling rate of the filter structure in accordance with $R \leq 1/2$.

With the FIR filter structure in accordance with the invention shown in Figure 3, the decimator 2 reduces the input sampling rate f_a by the fractional sampling rate change factor $R = L/M < 1$. The sampling rate for the

core filter 1 thus results as $f_k = f_a*L/M$. In the decimator 2, the input signal for the core filter 1 must be expanded by the factor L with the transfer function D' = D'(z) in stage 21, must subsequently be band limited (stage 22 with the transfer function H) to suppress image frequency effects and aliasing effects and must then be compressed with the factor M in stage 23. The post-processing of the output signal of the core filter 1, in particular the regaining of the original input sampling frequency f_a, is carried out by operations which are transposed for input side expansion and compression (stages 31 and 33 of the interpolator 3). The filter structure in accordance with Fig. 3 can be used in the whole range of filter cut-off frequencies $f_S \in (0, f_a/2)$.

The structure shown in Figure 4a is suitable for reducing computing effort. In particular ML parallel filter paths for parallelized part systems are provided there. (Such a parallelized FSRC is shown in Figure 4b). The filter functions H and G are formed in poly-phase structure. Both the decimator 2 and the interpolator 3 are set to operate at a uniform sampling rate $f_k = f_a/M$ with respective ML poly-phase part components. It is advantageous to design the whole filter such that all sub-systems, i.e. decimator part systems and interpolator part systems as well as the core filter 1 operate with the uniform sub-Nyquist sampling rate $f_k = f_a/M$.

Starting from the realization in accordance with Figure 4, the input of the core filter 1 is associated with the transfer function D'(z) via an L to 1 commutator 4 for an L-times sampling rate expansion, cf. also example in accordance with Figure 5. The commutator 4 samples the L filter paths of the decimator 3 cyclically in accordance with the realization in accordance with US 4,725,972 and directs these sampled signals to the input of the

core filter 1. The output of the core filter 1 is connected to a 1 to L commutator (distribution multiplexer) 5, that is to a dual structure with respect to the L to 1 commutator 4 for an L-times sampling rate reduction and parallelization.

To achieve a lower sampling frequency for the core filter 1, it is necessary to transpose the sequence of expansion components and core filter components or step-down samplers and core filter components. For this purpose, the transfer function D'(z) of the core filter 1 is included in the parallel filter paths of the decimator 2, as shown in Figure 6, or in a variant (not shown) in the parallel filter paths of the interpolator. For this, delayed versions of $D'_{(z)}$ are defined which correspond to time-displaced pulse responses $D'_{(v)}$:

$$D'_{\nu}(z) = z^{-\nu} D'(z) \overset{zT}{\underset{\Leftrightarrow}{}} d'_{\nu}(n) = d'(n-\nu).$$

The transposition of the expanders and of the delayed versions of the core filter 1 $D'_v(z)$ is possible by means of equivalence relationships which have been termed "noble identities". For this purpose, the filters $D'_v(z)$ are broken down into respective L poly-phase components $D'_v\lambda(z^L)$ in accordance with

$$D'_{\nu}(z) = \sum_{\lambda=0}^{L-1} z^{-\lambda} D'_{\nu\lambda}(z^L) = \sum_{\lambda=0}^{L-1} z^{-\lambda} D'_{\nu\lambda}(z')$$

where λ = 0, ..., L-1. Subsequently, a displacement of the expanders by means of the "noble identifiers" is possible. The results are L poly-phase interpolators (or poly-phase decimators) with identical commutators which

can be combined to a single one by elementary conversion. After this conversion, the structure shown in Figure 7 arises which shows the two commutator switches 4 and 5 for a cyclic sampling in accordance with the decimator structure 2 with L parallel paths which are directly connected in cascade and have the same number of parallel paths.

In Figure 7a, each transfer function $D'_p(l)(z^L)$ for $1 = 0, \ldots, L-1$ represents all L poly-phase components of the index L of the delay filters $D'_\nu(z)$ for each $\nu = 0, \ldots, L-1$. The different transfer functions are shown in more detail in Figure 7b. The commutators 4 and 5 can be omitted with a suitable technical circuit linkage (rearrangement) of corresponding parallel paths. In the final structure derived in this manner, the core filter 1 and/or the L phase components and the decimation filter paths 2 and the interpolation filter paths 3 operate with the uniform sampling frequency $f_k = f_a/M$. The condition:

$$2f_{max} \leq L/M*f_a$$

must be observed to satisfy the sampling theory, for example, for low pass signals. Since all part filters operate with the sampling frequency f_a/M, the whole signal processing is carried out at a sub-Nyquist sampling rate.

The sampling rate change factor $R = L/M$ is preferably selected such that it lies as close as possible to the optimum sampling rate change factor R_{opt} shown in Figure 2 which can be determined analytically beforehand.

Once the optimum sampling rate change factor R_{opt} has been set, the sampling rate for parallelized filter paths can be set as desired by a varia-

tion of the numbers M and L in the same sense, without the overall computing effort changing.

In this case, L = int(R_{opt}*M) applies, where int(R_{opt}*M) designates the integer value which lies closest to Ropt*M. A pre-condition is that L and M are aliquant (have no common divisor). This leads to a filter structure in accordance with Figure 8.

For an example, an input sampling frequency f_a of 800 MHz was selected. A value of 16/25 was determined as the optimum sample rate change factor R_{opt} = L/M with a pre-set tolerance scheme (δ_D, δ_s) and the pre-set limit frequencies of the transmission range and cut-off range Ω_D and Ω_s. The uniform sub-Nyquist sampling rate for the filter paths thus results as f_k = 32 MHz.

The fractional sampling rate conversion underlying the invention has up to now been presented as a single stage procedure. It is already known from [1] (page 147 – 149) that a multi-stage integer-based sampling rate conversion is more favorable as regards effort than a single stage integer-based conversion. Instead of the multi-stage integer-based sampling rate conversion used in [1], a multi-stage fractional sampling rate conversion would be more favorable as regards effort, since the optimum sampling rate change factors R_i can be better approximated with I = stage number.

An output commutator 7 and an input commutator 8 are interposed between each stage by the cascading of a plurality of FSRCs made in a computation efficient structure. If an elimination of the switches is desired, then this is only possible when both switches have the same branch

number, i.e. $L_i = M_{i+1}$. Additional I-1 conditions, where I = stage number, are thus given overall, and the new search area, in which the effort minimum is sought, is only a part of the original area. If the solution, which resulted without the additional conditions, is no longer part of this new solution area, then a new solution results with a higher effort than the minimum effort.

A parallelization is again also possible here through the inclusion of the core filter into the adjacent decimator or interpolator and results in the elimination of the inner commutators.

CLAIMS

1. A filter device consisting of a core filter (1) and also of a decimator (2) at the input side and of an interpolator (3) at the output side, with the following features:

- the decimator (2) is designed to realize a reduction in the input sampling rate f_a of the filter device by a fractional sampling change factor $L/M < 1$, where L and M are natural numbers;

- the core filter (1) is designed to carry out the filtration at the sampling rate reduced in this manner;

- the interpolator (3) is designed to raise the sampling rate of the core filter (1) again to the original input sampling rate f_a.

2. A filter device in accordance with claim 1, characterized in that respective parallel filter paths are provided for the decimator (2) and/or the interpolator (3) which can be sampled cyclically.

3. A filter device in accordance with claim 1 or claim 2, characterized in that the core filter (1) is converted into L differently time-delayed filters which are broken down into poly-phase components so that it can be combined with the decimator (2) or the interpolator (3).

4. A filter device in accordance with any one of claims 1 to 3, characterized in that the system equivalent to the core filter (1) can be operated with a clock rate of f_a/M.

5. A filter device in accordance with any one of claims 2 to 4, characterized in that the decimator (2) or the interpolator (3) are rearranged relative to the parallel paths with respect to the poly-phase components of the core filter (1) such that the normally necessary commutators (4, 5) for forwarding sampling values to the core filter (1) can be omitted.

6. A filter device in accordance with any one of claims 1 to 5, characterized in that both the decimator (2) and the interpolator (3) as well as, optionally, the core filter (1) are set to be operated at a uniform sampling rate.

7. A filter device in accordance with any one of claims 1 to 6, characterized in that an optimum is selected for the sampling rate change factor R = L/M at which a minimum of computing effort arises for the digital filtering, with this computing effort in particular being characterized as filter operations per unit of time.

8. A filter device in accordance with claim 7, characterized in that, with the optimum sampling rate change factor R = L/M, any desired sampling rates can be set for the parallelized filter paths of the decimator (2), of the interpolator (3) and of the core filter phase components (1) by a variation of the numbers L and M in the same sense.

9. A filter device in accordance with any one of claims 1 to 8, characterized in that FIR filter structures, in particular of a non-recursive

kind, are used for the core filter (1) and for the decimator (2) and the interpolator (3).

10. A filter device consisting of a plurality of cascaded stages, characterized in that every stage is formed as a filter device in accordance with any one of claims 1 to 3.

11. A filter device in accordance with claim 10, characterized in that the filter device has a central stage which is formed in accordance with any one of claims 4 to 9.

(12) NACH DEM VERTRAG ÜBER DIE INTERNATIONALE ZUSAMMENARBEIT AUF DEM GEBIET DES PATENTWESENS (PCT) VERÖFFENTLICHTE INTERNATIONALE ANMELDUNG

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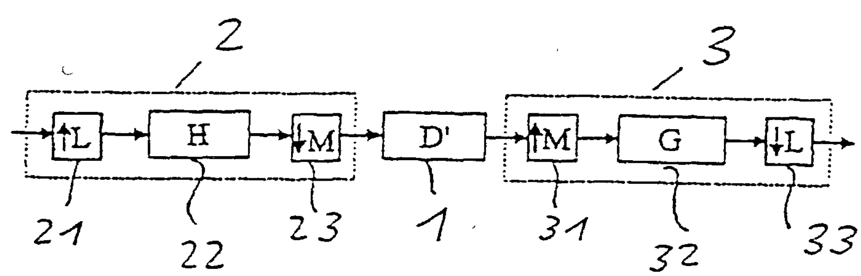
(84) **Bestimmungsstaaten** *(regional)*: ARIPO-Patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), eurasisches Patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), europäisches Patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI-Patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Veröffentlicht:
— *Mit internationalem Recherchenbericht.*
— *Vor Ablauf der für Änderungen der Ansprüche geltenden Frist; Veröffentlichung wird wiederholt, falls Änderungen eintreffen.*

Zur Erklärung der Zweibuchstaben-Codes, und der anderen Abkürzungen wird auf die Erklärungen ("Guidance Notes on Codes and Abbreviations") am Anfang jeder regulären Ausgabe der PCT-Gazette verwiesen.

(54) **Title:** FILTER UNIT COMPRISING A CORE FILTER, DECIMATOR AND INTERPOLATOR

(54) **Bezeichnung:** FILTEREINRICHTUNG MIT KERNFILTER, DEZIMATOR UND INTERPOLATOR



(57) **Abstract:** The invention relates to a filter unit, comprising a decimator (2), core filter (1) and an interpolator (3). According to the invention, the sampling rate is decreased by a fractional sampling rate modification factor L/M, prior to the core filtration process. This allows the construction of a simple filter structure which can be universally used. Parallelisation achieves a structure whose clock rate can be freely modified.

(57) **Zusammenfassung:** Bei einer Filtereinrichtung bestehend aus Dezimator (2), Kernfilter (1) und Interpolator (3) wird eine Verminderung der Abtastrate um einen nicht ganzzahligen Abtastratenänderungsfaktor L/M vorgenommen, bevor die Kernfilterung erfolgt. Es lässt sich damit eine Filterstruktur mit geringem Aufwand realisieren, die universell einsetzbar ist. Durch eine Parallelisierung wird eine Struktur erzielt, deren Taktrate frei einstellbar ist.

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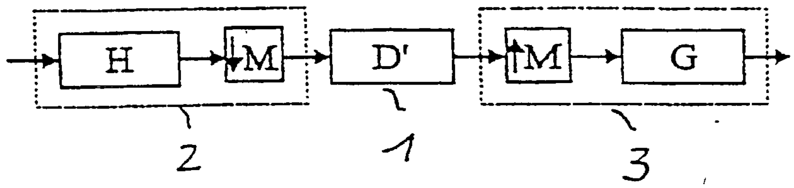

Fig. 1

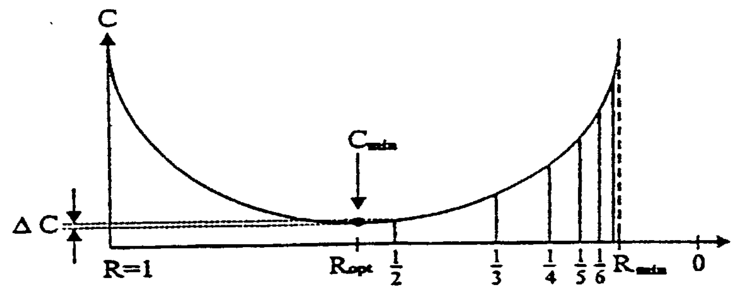

Fig. 2

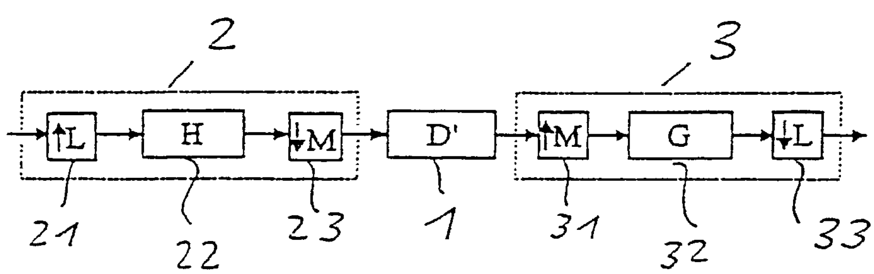

Fig. 3

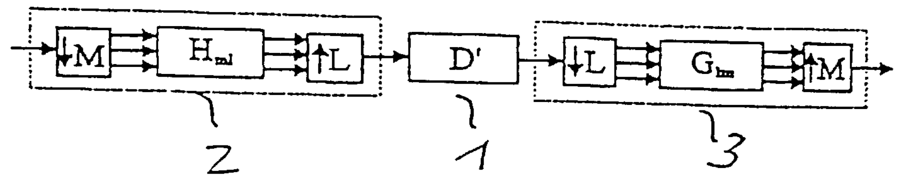

Fig. 4a

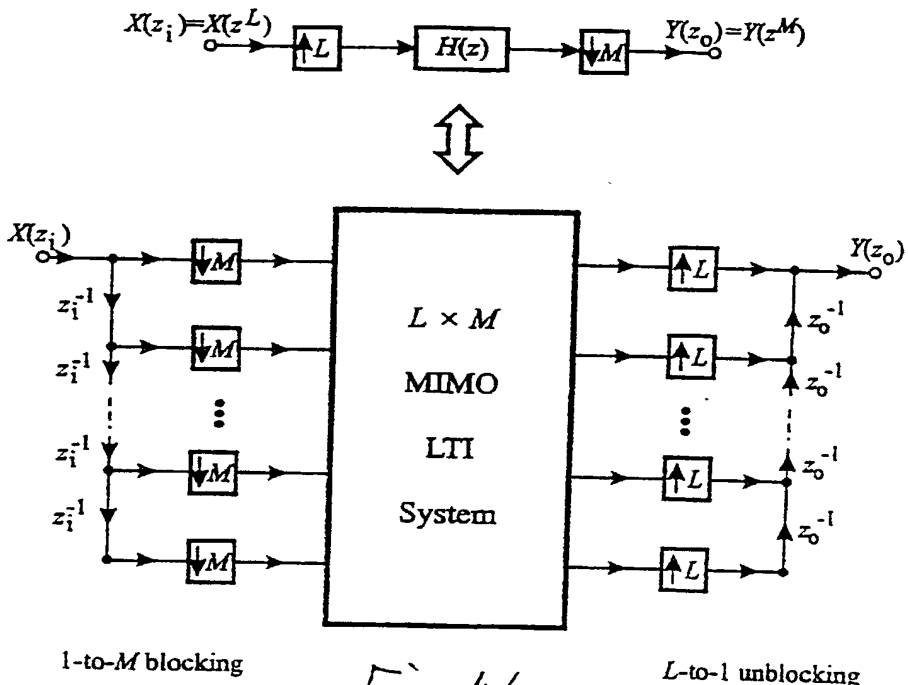

Fig. 4b

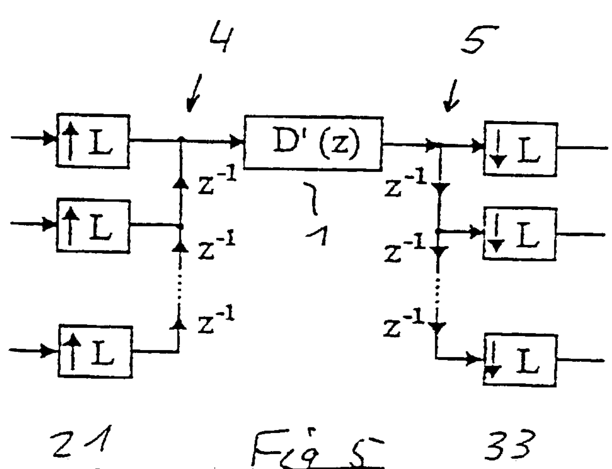

Fig. 5

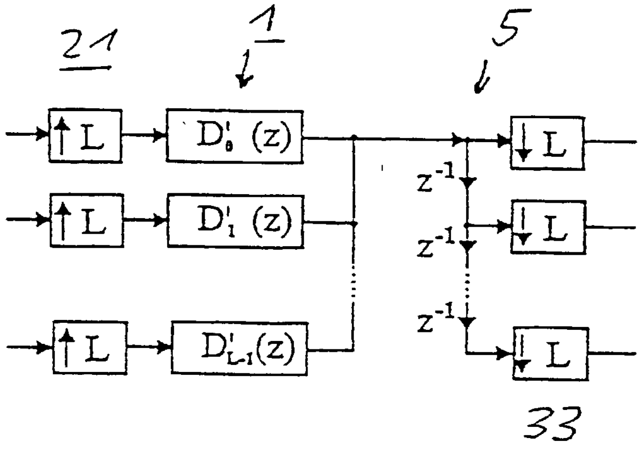

Fig. 6

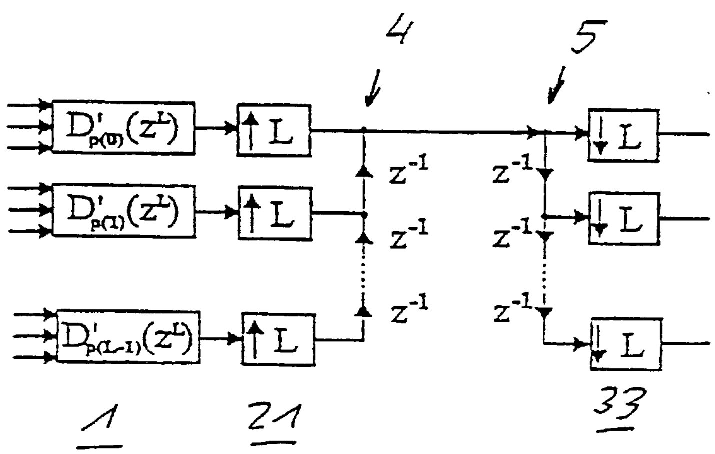

Fig. 7a

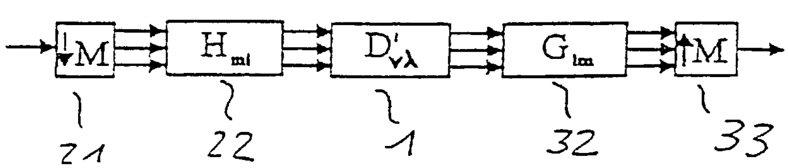

Fig. 8

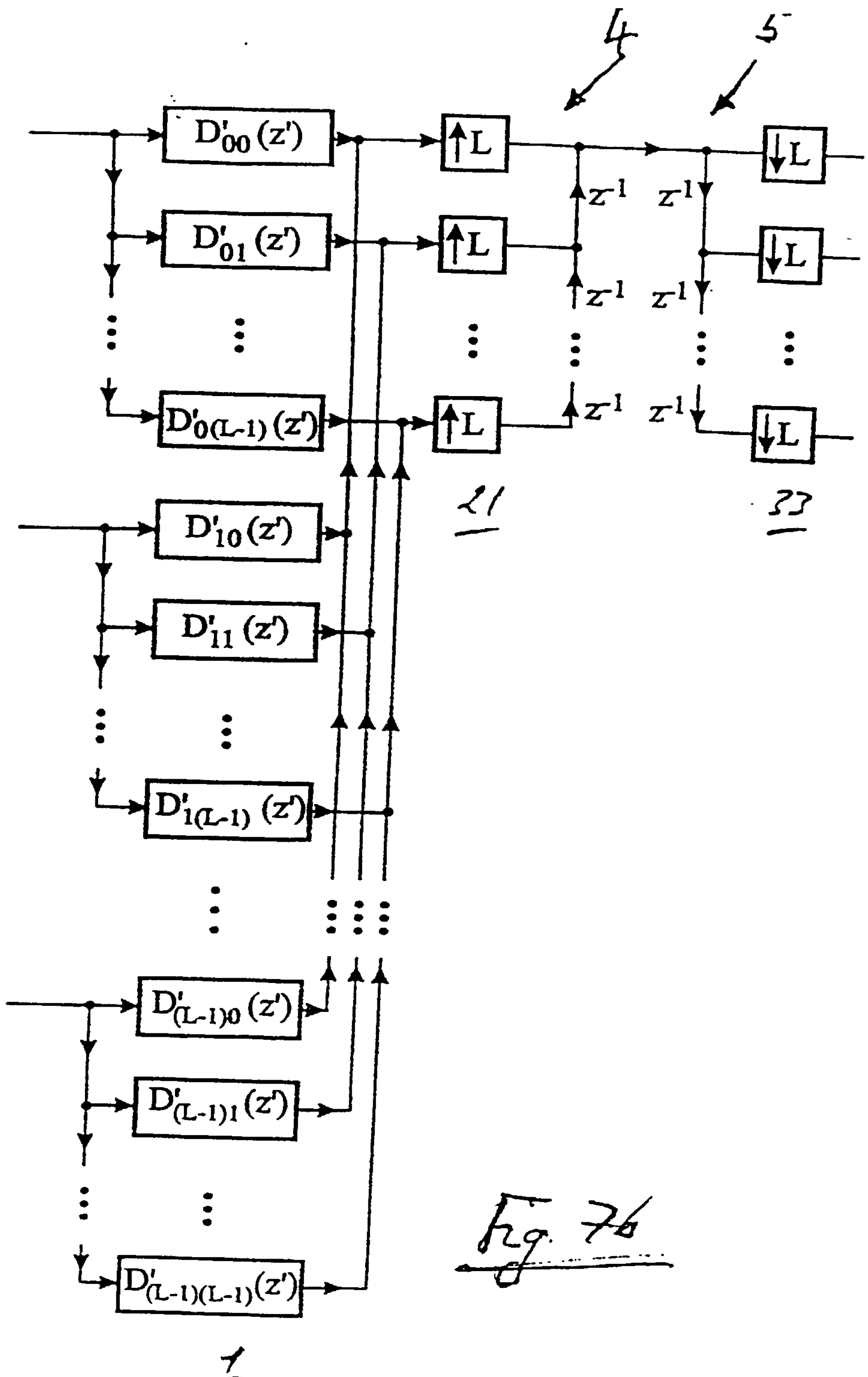
4
5
$D'_{00}(z')$
$D'_{01}(z')$
$D'_{0(L-1)}(z')$
$D'_{10}(z')$
$D'_{11}(z')$
$D'_{1(L-1)}(z')$
$D'_{(L-1)0}(z')$
$D'_{(L-1)1}(z')$
$D'_{(L-1)(L-1)}(z')$
↑L
↓L
z^{-1}
21
33
1

Fig. 7b

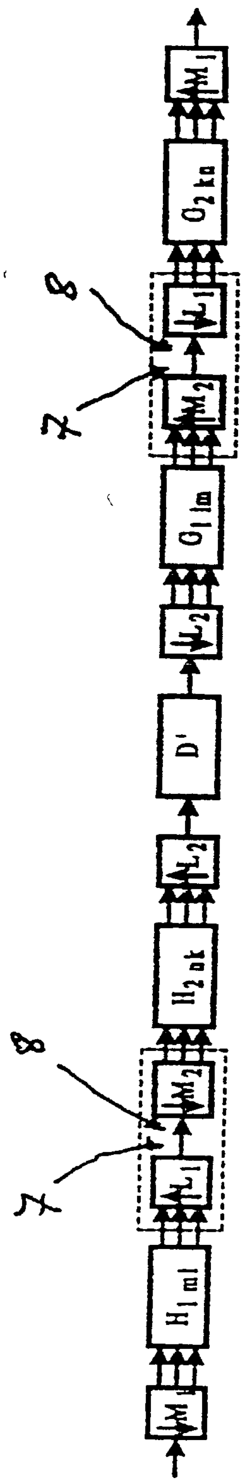

Fig. 9

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PCT/USA NATIONAL DECLARATION AND POWER OF ATTORNEY
FOR U.S. PATENT APPLICATIONS
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
UNDER 35 U.S.C. SECTION 371(c)(4)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name:

I verily believe I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the invention described and claimed in international application No. PCT/IB00/01306 entitled: FILTER DEVICE COMPRISING A CORE FILTER, A DECIMATOR AND AN INTERPOLATOR, and as amended on ______________ (if any), which I have reviewed, and I understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above and for which I solicit a patent; that I do not know and do not believe that this invention was ever known or used in the United States of America before my or our invention or discovery thereof, or patented or described in any printed publication in any country before my or our invention or discovery thereof, or more than one year prior to my international application; that this invention was not in public use or on sale in the United States of America for more than one year prior to my international application; that this invention has not been patented or made the subject of an inventor's certificate issued before the date of my international application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months before my international application; that I acknowledge my duty to disclose information of which I am aware which is material to the examination of this application; and that prior to filing said international application, applications for patent or inventor's certificate on this invention of discovery which have been filed by me or my legal representatives or assigns in any country foreign to the United States of America are as follows:

(a) none filed more than 12 months prior to said international application, unless named below:

(b) earliest filed less than 12 months prior to said international application (the priority of which is hereby claimed under 35 U.S.C. Section 365):

DE 199 40 926.9 filed August 27, 1999.

I hereby claim the benefit under Title 35, United States Code, §120, of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a), which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

______________	______________	______________
(Application Serial No.)	(Filing Date)	(Status)(patented, pending, abandoned)

(4) I hereby appoint Todd T. Taylor, Reg. No. 36,945; Ronald K. Aust, Reg. No. 36,735; Keith J. Swedo, Reg. No. 43,176 and Jeffrey T. Knapp, Reg. No. 45,384, of the firm of TAYLOR & AUST, P.C., as attorney(s)/patent agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

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I declare further that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

1-00

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2-00

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